

FIG. 1 is a schematic diagram of a system for processing data. The system includes a plurality of input devices (1, 2, ..., N) connected to a central processing unit (HE) via a bus (10). The central processing unit (HE) is connected to a memory unit (L20) via a bus (20). The memory unit (L20) is connected to an output device (20) via a bus (20).

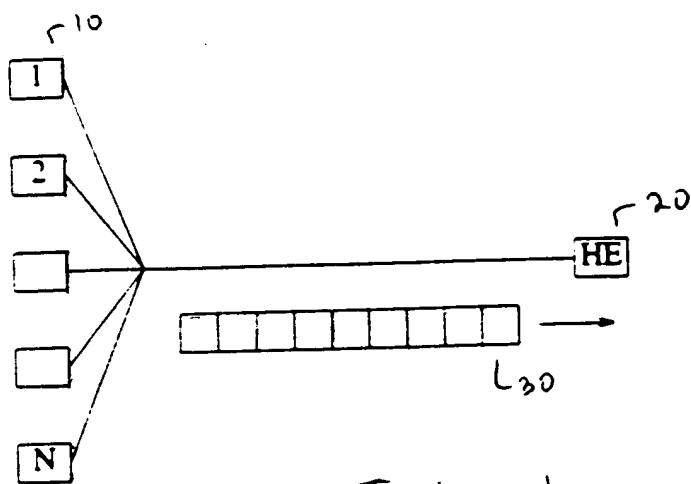


FIG. 1

The first time slot is the first time slot in the queue. The first time slot is the first time slot in the queue. The first time slot is the first time slot in the queue.

Time Instant	# of Arrivals	# of Slots from Headend	Queue Size	# of Slots Requested
t=0	0	0	12	12
1	0	0	12	12
2	0	0	12	12
3	0	12	0	0
4	0	12	0	0
5	0	12	0	0
6	0	0	0	0
7	0	0	0	0
8	0	0	0	0
9	0	0	0	0

Number of Wasted Slots

24

Figure 2

The first row shows the initial state of the system at $t=0$. The second row shows the state after the first arrival. The third row shows the state after the second arrival. The fourth row shows the state after the third arrival. The fifth row shows the state after the fourth arrival. The sixth row shows the state after the fifth arrival. The seventh row shows the state after the sixth arrival. The eighth row shows the state after the seventh arrival. The ninth row shows the state after the eighth arrival. The tenth row shows the state after the ninth arrival.

Time Instant	# of Arrivals	# of Slots from Headend	Queue Size	# of Slots Requested
$t=0$	0	0	12	4
1	0	0	12	4
2	0	0	12	4
3	0	4	8	3
4	0	4	4	2
5	3	4	3	3
6	0	3	0	0
7	0	2	0	0
8	0	3	0	0
9	0	0	0	0

Number of Wasted Slots

5

Figure 4